

### REMARKS

Claim 1 was rejected under Section 102 as being anticipated by Kitamura. It is indicated that Kitamura teaches a mathematical processor, namely element 5, in Figure 6. However, as indicated in column 11 of Kitamura, paragraph 39, beginning at line 47, the data processing unit 5 splices the video data DA and DB in response to a splicing instruction from CPU 7. There is absolutely no indication that this device can be considered to be a mathematical processor. Thus, at least one element is missing in Kitamura and, therefore, the Section 102 rejection is subject to being withdrawn.

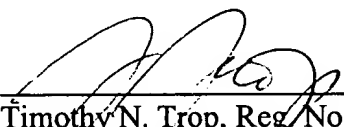
Similarly, claim 16 calls for using a third processor for mathematical operations. No such thing is shown in Kitamura.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested.

Respectfully submitted,

Date: \_\_\_\_\_

8/9/02

  
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## **APPENDIX**

### **IN THE SPECIFICATION**

Please amend the paragraph beginning on page 5, line 1, as follows:

The programmable random access memory (RAM) processor (PRP) [20] 24 basically stores and retrieves data. It may be particularly advantageous in storing intermediate results, in a cache-like fashion. This may be particularly applicable in two-dimensional image processing.

### **IN THE DRAWINGS**

The proposed drawing corrections are indicated in red on the attached sheets.

### **IN THE CLAIMS**

Please cancel claims 25-30.

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DATA FROM ANY PROCESSOR

GPR 0

DATA OUT

CHAINING SOC DEFINED BY INPUT BY ANY PROCESSOR WRITES EXCEPT INPUT PROCESSOR WRITES

GPR 1

DATA OUT

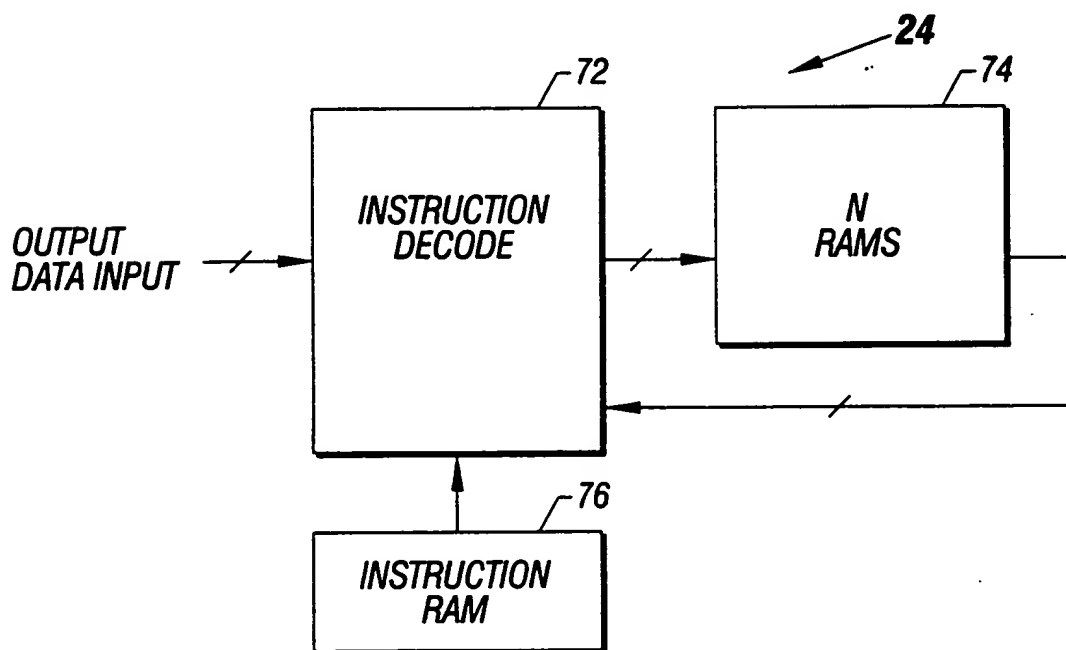
PROGRAMMABLE END OF CHAIN

\* \* \* \* \*

GPR N

DATA OUT

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**FIG. 7**



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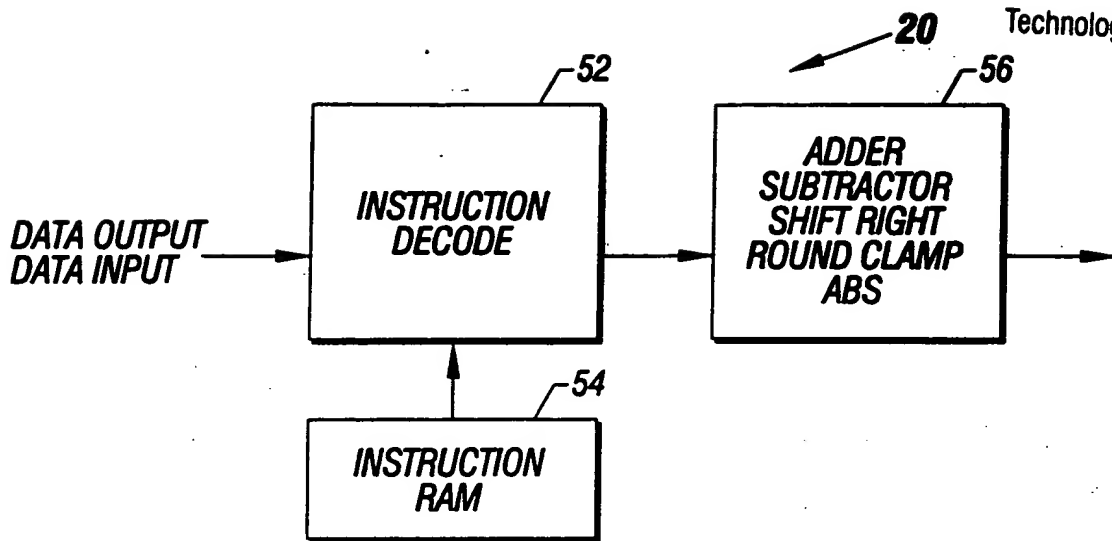


FIG. 4

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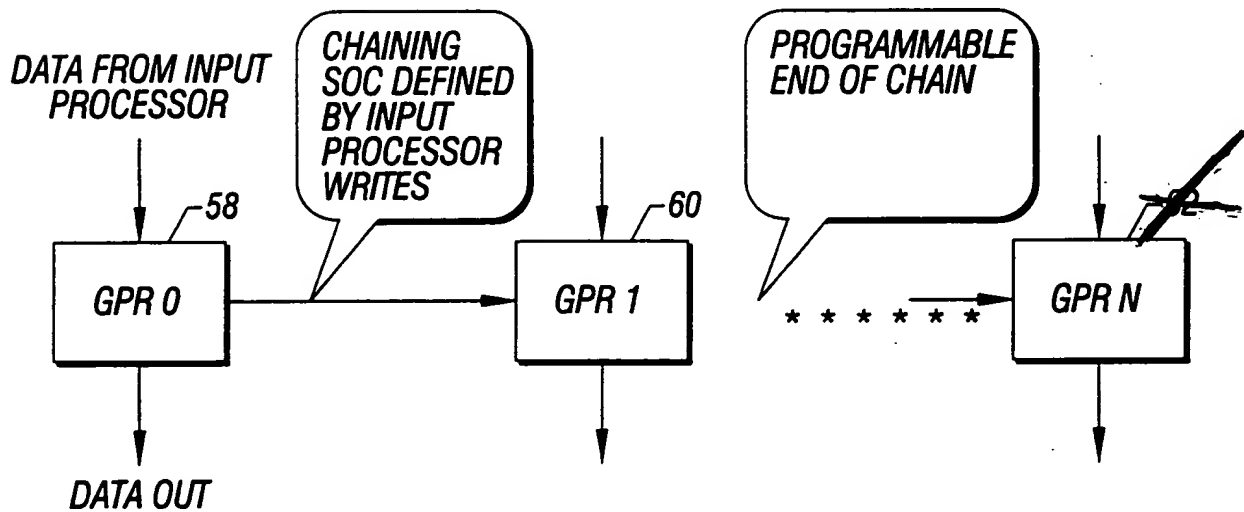


FIG. 5



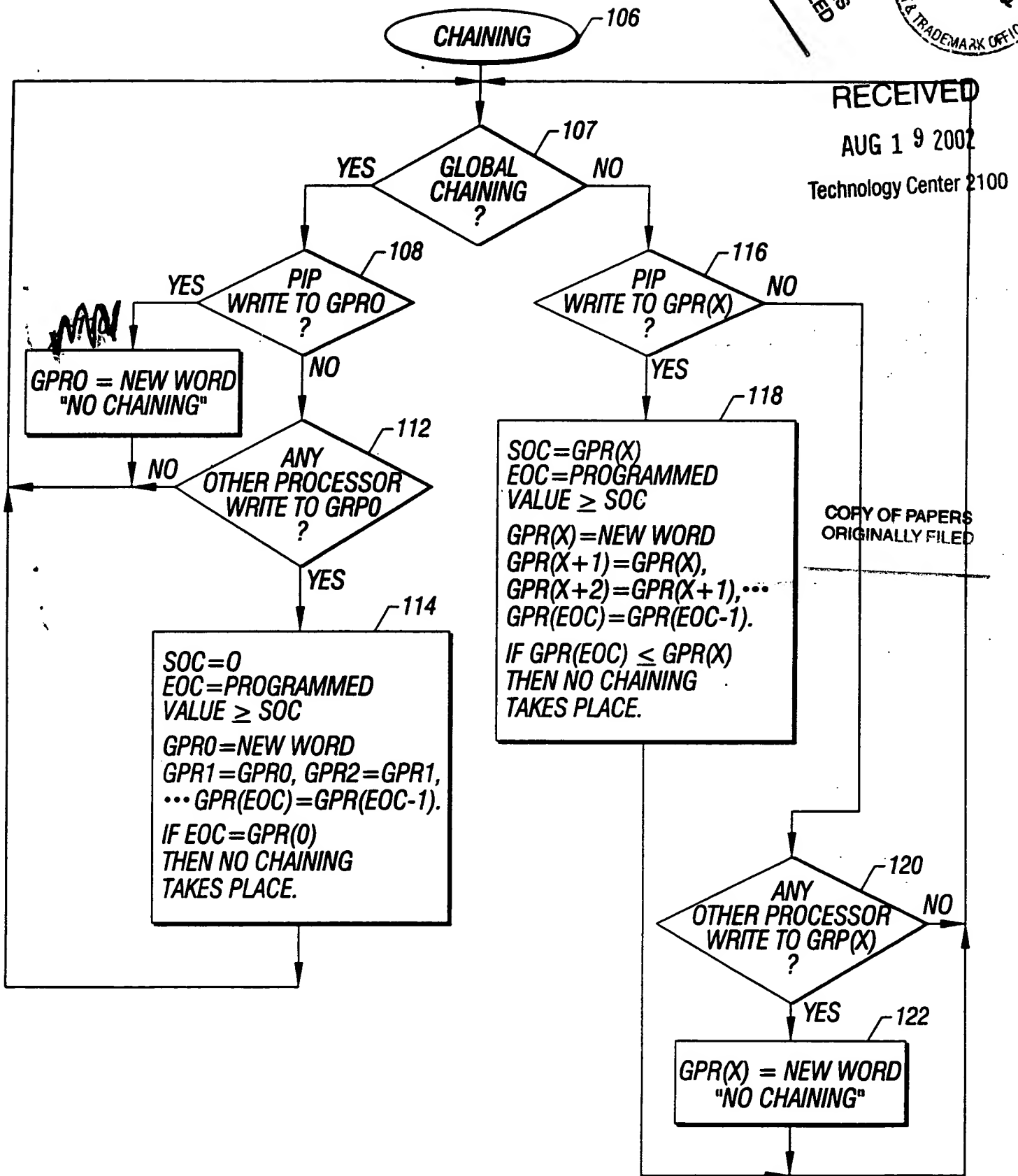


FIG. 13